

**REMARKS**

Claims 1-8 are in the present application pending. Claim 8 has been added herein.

**I. PRIOR ART REJECTION**

The Examiner has rejected claims 1-7 under 35 U.S.C. § 102(a) as anticipated by U.S. Patent No. 6,025,822 (Motegi). This rejection is traversed.

**A. Claims 1-5:**

The characterizing feature of claims 1-5 is that the plurality of column electrode driving circuits is connected in series, i.e., the input of a second column electrode driving circuit is connected to the output of a first column electrode driving circuit, and so on, and hence the timing signals are passed between the column electrode driving circuits in a cascade manner.

The Examiner asserts that the liquid crystal driving circuit 14 in Fig. 4 of Motegi, et al. is connected to the data input section of another column electrode driving circuit. Applicant respectfully submits that this assertion is not correct for the following reasons:

Firstly, the entire section 111 of Fig. 4 of Motegi, et al. is a single column electrode driving circuit, which receives input only from the RGB signal input, the row data generating circuit 41 and the column controller 2. The only output 17 of the column electrode driving circuit is connected to the column electrodes in the display panel (as described at col. 9, lines 43-44 of Motegi). That is, the outputs of each of the plurality of column electrode driving circuits are not

connected to the inputs of another of the column electrode driving circuits (in series) at all.

Further, with reference to Fig. 7 of Motegi, the column electrode driving circuits 21 are not connected to each other in series, but are connected in parallel. This is completely the opposite configuration to that of the present invention, which can be seen graphically in Figure 2 of the present application.

Therefore, since Motegi does not teach or suggest each and every feature of claims 1-5, Applicant submits that these claims are not anticipated by Motegi. Therefore, the rejection of claims 1-5 under 35 U.S.C. § 102(a) is improper and should be withdrawn.

#### B. Claims 6 and 7

One feature of claims 6 and 7 is that the timing signal is supplied from a first column electrode driving circuit to a first row electrode driving circuit via a specific path as follows:

Sequentially through a first line portion provided on the tape carrier package mounting the first column electrode driving circuit, a second line portion provided on the printed circuit board, a third line portion provided on the tape carrier package mounting the first column electrode driving circuit, and a fourth line portion provided on the display panel.

The Examiner has asserted that this configuration is disclosed in Motegi. However, the Examiner has failed to identify any specific section of Motegi, either in the figures or specification, to support this contention. Applicant respectfully submits that Motegi does not disclose such configuration.

Further, Applicant submits that Motegi does not teach or suggest that the row and column electrode driving circuits are arranged in line, as recited by claims 6 and 7. This feature is shown in Figure 3B of the present application.

Therefore, since Motegi does not teach or suggest each and every feature of claims 6-7, Applicant submits that these claims are not anticipated by Motegi. Therefore, the rejection of claims 6-7 under 35 U.S.C. § 102(a) is improper and should be withdrawn.


Regarding new claim 8, Applicant submits that the features of this claim are not taught or suggested by Motegi.

Based on the foregoing, Applicant submits that the present application is in condition for allowance. Applicant kindly requests the Examiner to contact the undersigned at the phone number listed below to discuss this application, if the Examiner feels that such discussion may expedite prosecution of the present application.

Applicant believes that no additional fees are due for the subject application. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. 04-1105.

Respectfully Submitted,

Date: 7/17/03  
Customer No.: 21874

  
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IN THE CLAIMS:

8. (Added) A matrix type display device, comprising:
- a display panel;
  - a plurality of column electrode driving circuits arranged in a line on a circuit board provided along a first side of the display panel; and
  - a plurality of row electrode driving circuits arranged in a line and provided along a second side of the display panel, the second side being adjacent to the first side,
- wherein,
- a first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, generates a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits, and outputs the generated timing signal to a first row electrode driving circuit, among the plurality of row electrode driving circuits, which is closest to the first column electrode driving circuit as a scanning signal,
  - a signal circuit is provided to use for signals being different from a timing signal which is output from the first column electrode driving circuit, and
  - the timing signal which is output from the first column electrode driving circuit is supplied to the first row electrode driving circuit sequentially through the circuit board so as not to be crossed with the signal circuit.